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10/020,019	12/07/2001	Francesco Pessolano	NL 000667	8972

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PHILIPS INTELLECTUAL PROPERTY & STANDARDS
P.O. BOX 3001
BRIARCLIFF MANOR, NY 10510

EXAMINER	
PETRANEK, JACOB ANDREW	
ART UNIT	**PAPER NUMBER**
2183	

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12/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/020,019	PESSOLANO ET AL.	
	Examiner	Art Unit	
	Jacob Petranek	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 October 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-11,13 and 14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-11,13 and 14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-3, 5-11 and 13-14 are pending.

2. The office acknowledges the following papers:

Claims and arguments filed on 10/2/2007.

New Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-2, 5-9, 11, and 13-14 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites "wherein each functional unit has a private control unit for controlling function of an associated functional unit." It's unclear what "an associated function unit" is supposed to be. For purposes of example, looking at figure 5 in the drawings, a private control unit is local control (process A). It's unclear if the associated functional unit is to be the execution element directly under the local control (process A) element or if the associated functional unit can be any of the execution elements in figure 5. For examination purposes, an associated functional unit will be interpreted as execution element directly under its corresponding private control element.

5. Claims 2, 5-9, 11, and 13-14 are rejected due to their dependency.

New Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-3, 5-11 and 13-14 are rejected under 35 U.S.C. §103(a) as being unpatentable over Masse et al. (U.S. 6,990,570), in view of Ganapathy et al. (U.S. 6,598,155), in view of Redford (U.S. 6,732,253).

8. As per claim 1:

Masse disclosed a digital signal processing apparatus for executing a plurality of operations in a loop, comprising:

A functional unit wherein the functional unit is adapted to execute operations (Masse: Figure 10 element 904, column 11 lines 13-18),

And control means for controlling said functional unit characterized in that said control means comprises a fetch unit, a decode unit, and a control unit responsive to said decode unit (Masse: Figure 10 elements 918 and 932, column 10 lines 1-18 and column 11 lines 1-33)(Elements 918 and 932 make up the control unit that is coupled to the functional unit. Official notice is given that the instructions executed by processors are fetched and decoded. Thus, it's obvious to one of ordinary skill in the art that the computed single repeat instruction is fetched from a fetch unit and decoded by a decode unit. The decode unit tells the control unit of figure 10 that the instruction is a repeat instruction, which causes it to be repeated according to the counter element.),

Wherein the functional unit has a private control unit for controlling function of an associated functional unit, including controlling a number of repetitions of execution of the function (Masse: Figure 10 elements 918, 922, and 932, column 11 lines 23-33)(Elements 922 and 932 control the number of repetitions of the repeat instruction. The ALU has its own private control unit in elements 918, 922, and 932.),

And each functional unit is adapted to execute operations in an autonomous manner under private control of the control unit associated therewith so that access to an external instruction memory is reduced (Masse: Figure 10 elements 904, 918, 922, and 932, column 11 lines 1-33)(A repeat instruction inherently reduces accesses to external memory by reducing the number of instructions that need to be fetched within a program. The control logic allows for the repeated execution of the repeat instruction according to the count value by the ALU.),

Including transfer of control to the control means upon completion of an operation included in the loop and execution of instructions of a subsequent loop instead of being stalled or executing a no-operation instruction (Masse: Figure 10 elements 926, 930 and 932, column 11 lines 23-33)(Upon exiting the repeat instruction, it's obvious to one of ordinary skill in the art that execution would want to be continued as opposed to stalling or executing no-ops for the advantage of increased performance through increased throughput. Official notice is given that a prefetch mechanism could be added to prefetch instructions after the repeat instruction. Thus, since instructions are already within the instruction cache at the exit of the repeat instruction, it's obvious to one of ordinary skill in the art that these instructions can be fetched and executed instead of

stalling or executing no-ops. In addition, it's obvious to one of ordinary skill in the art that a program could execute nested loops, which results in upon exiting one loop, another loop is entered.),

Wherein each private control unit includes a counter indicating how often the one operation or the sequence of operations still has to be executed (Masse: Figure 10 element 922, column 11 lines 23-33).

Masse failed to teach a plurality of functional units wherein each functional unit is adapted to execute operations; the plurality of function units has a private control unit; and wherein each private control unit includes an instruction memory configured to hold one operation or a sequence of operations.

However, Ganapathy disclosed wherein each private control unit includes an instruction memory configured to hold one operation or a sequence of operations (Ganapathy: Figure 8a element 710A, column 15 lines 63-67 continued to column 16 lines 1-13)(The combination results in the loop buffer storing the repeat instructions of Masse to feed into the ALU directly.).

Masse disclosed that a repeat instruction can be directly fed into a functional unit, but failed to disclose how the instruction itself is stored within the processor. The instruction that feeds into the ALU of Masse inherently must be stored within the processor itself. This would have motivated one of ordinary skill in the art to combine a known method in the prior art of storing repeating or loop instructions within a special memory as shown in Ganapathy. Thus, one of ordinary skill in the art would have used

the loop buffer of Ganapathy to store the repeat instructions of Masse for the advantage of being able to repeatedly send the instructions into the ALU.

Masse and Ganapathy failed to teach a plurality of functional units wherein each functional unit is adapted to execute operations and the plurality of function units has a private control unit.

However, Redford disclosed a plurality of functional units wherein each functional unit is adapted to execute operations and has a private control unit (Redford: Figure 1 element 18, column 2 lines 61-65)(Official notice is given that SIMD processors contain multiple functional units to execute a single instruction on multiple data in parallel. Thus, it's obvious to one of ordinary skill in the art that each datapath has a functional unit to execute the single operation with different data. The combination results in the control unit of Masse and Ganapathy being used for each individual functional unit of Redford. This allows for operations to be repeated by each functional unit.).

The advantage of SIMD processors is that they are able to efficiently processor arrays of data items (Redford: Column 1 lines 12-30). One of ordinary skill in the art would have been motivated by this advantage to implement SIMD onto the processor of Masse. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement SIMD processing on the processor of Masse for the advantage of efficiently processing arrays of data items.

9. As per claim 2:

Masse, Ganapathy, and Redford disclosed an apparatus according to claim 1, characterized by FIFO (first-in/first-out) register means adapted for supporting data-flow

communication among said functional units (Ganapathy: Figure 7 element 710, column 13 lines 30-38 and lines 60-64)(The loop buffer is a FIFO type buffer containing registers to store instructions.).

10. As per claim 3:

Claim 3 essentially recites the same limitations of claim 5. Therefore, claim 3 is rejected for the same reasons as claim 5.

11. As per claim 5:

Masse, Ganapathy, and Redford disclosed an apparatus according to claim 2, characterized in that said FIFO register means comprises a plurality of FIFO registers (Ganapathy: Figure 7 element 710, column 13 lines 30-38 and lines 60-64)(The loop buffer is a FIFO type buffer containing registers to store instructions.).

12. As per claim 6:

Masse, Ganapathy, and Redford disclosed an apparatus according to claim 1, characterized in that each of said functional units are provided with at least one control unit (Redford: Figure 1 element 18, column 2 lines 61-65)(Official notice is given that SIMD processors contain multiple functional units to execute a single instruction on multiple data in parallel. Thus, it's obvious to one of ordinary skill in the art that each datapath has a functional unit to execute the single operation with different data. The combination results in the control unit of Masse and Ganapathy being used for each individual functional unit of Redford. This allows for operations to be repeated by each functional unit.).

13. As per claim 7:

Masse, Ganapathy, and Redford disclosed an apparatus according to claim 1, which apparatus is adapted to form a pipeline consisting of a plurality of stages, wherein each stage comprises a functional unit (Official notice is given that pipelined processors comprise a plurality of stages, each having a unit to perform a given function. Such given functions can be fetching, decoding, and executing instructions, to name a few. Thus, it's obvious to one of ordinary skill in the art that the processor of Masse is a pipelined processor.).

14. As per claim 8:

Masse, Ganapathy, and Redford disclosed an apparatus according to claim 1, characterized in that for each control unit an instruction register and a counter are provided, wherein said counter indicates the number of times an instruction stored in said instruction register has to be executed by the corresponding functional unit (Masse: Figure 10 element 922, column 11 lines 23-33)(Ganapathy: Figure 8a element 710A, column 15 lines 63-67 continued to column 16 lines 1-13)(The combination results in the loop buffer storing the repeat instructions of Masse to feed into the ALU directly. The counter indicates the number of times instructions in the loop buffer are executed.).

15. As per claim 9:

Masse, Ganapathy, and Redford disclosed an apparatus according to claim 1, further comprising a program memory means storing a main program, characterized in that said main program contains directives for instructing said control units (Official notice is given that processors have both main memory and a hard disk memory, both of which store programs. Thus, it's obvious to one of ordinary skill in the art that the

processor of Masse has both a main memory and a hard disk memory to store a main program that is being processed currently by the processor. Instructions stored in these memories inherently contain opcodes that will tell the control units how to perform the given instruction in the processor.).

16. As per claim 10:

The additional limitation(s) of claim 10 basically recite the additional limitation(s) of claim 1. Therefore, claim 10 is rejected for the same reason(s) as claim 1.

17. As per claim 11:

The additional limitation(s) of claim 11 basically recite the additional limitation(s) of claim 2. Therefore, claim 11 is rejected for the same reason(s) as claim 2.

18. As per claim 13:

The additional limitation(s) of claim 13 basically recite the additional limitation(s) of claim 7. Therefore, claim 13 is rejected for the same reason(s) as claim 7. Examiner also notes that each of the stages is executed by a functional unit, e.g., the fetch unit is a functional unit because it's function is performing instruction fetches.

19. As per claim 14:

The additional limitation(s) of claim 14 basically recite the additional limitation(s) of claim 8. Therefore, claim 14 is rejected for the same reason(s) as claim 8.

Response to Arguments

20. The arguments presented by Applicant in the response, received on 10/2/2007 are considered persuasive.

21. Applicant argues "White and Tsushima either individually or in combination failed to teach wherein each private control unit includes an instruction memory configured to hold one operation or a sequence of operations, and a counter indicating how often the one operation or the sequence of operations still has to be executed" for claims 1, 3, and 10.

This argument is found to be persuasive for the following reason. The examiner agrees that none of the references either explicitly or inherently teaches the claimed limitation. However, a new ground of rejection has been given.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Batcher (U.S. 7,178,013), taught a repeat function with a counter.

Singh et al. (U.S. 6,898,693), taught processing hardware loops.

Fernando et al. (U.S. 6,269,440), taught processing a plurality of loop iterations at once.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Petranek whose telephone number is 571-272-5988. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jacob Petranek
Examiner, Art Unit 2183

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100